

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
 :
 Baydar et al :
 :
 Serial No.: To be assigned :
 :
 Filed: November 5, 2001 :
 :
 For: Integrated Digital Loop Carrier System :
 With Virtual Tributary Mapper Circuit :

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
 Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend the above-captioned application as follows:

IN THE SPECIFICATION:

Please substitute the following amended paragraph for the corresponding paragraph commencing on page 12, line 13 of the originally filed specification. A sheet is attached to provide a marked-up copy of the text indicating the proposed amendments thereto.

Figs. 49, 49A(i), 49(A)(ii) and 49B are a flow chart and state diagram illustrating a VT pointer interpretation algorithm in accordance with the present invention.

REMARKS

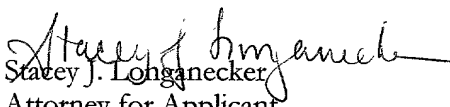
By the present amendment, the specification has been amended to correct typographical errors.

Claims 1-6 are pending. Claims 1-6 were originally numbered as claims 9-14 in the parent application Serial No. 08/471,224, filed June 6, 1995 (now issued as U.S. Patent No. 5,784,377).

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 T0907T-99958660

Claims 1-5 were indicated as being allowed in the Office Action dated September 3, 1996 in the parent application, but were not elected in that application. Claim 6 was also indicated as being allowable in the parent application, if amended to overcome a rejection under 35 U.S.C. § 112. Accordingly, claim 6 was amended in the paper submitted in the parent application on March 3, 1997 to overcome the rejection, but was not elected.

Respectfully Submitted,


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Figs. 49, 49A(i), 49(A)(ii) and 49B are a flow chart and state diagram[, respectively,] illustrating a VT pointer interpretation algorithm in accordance with the present invention.

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